UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,955	12/14/2001	Harry Chuang	TS01-1372	7559

28112 7590 06/19/2003

GEORGE O. SAILE & ASSOCIATES
28 DAVIS AVENUE
POUGHKEEPSIE, NY 12603

EXAMINER	
PHAM, THANHHA S	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 06/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,955	CHUANG, HARRY	
	Examin r	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-87* is/are pending in the application.

4a) Of the above claim(s) *78-87* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action responses to Applicant's Response in Paper No. 9 dated 04/07/03.

Election/Restrictions

1. Claims 78-67 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 9 dated 4/7/03.

2. Applicant's election with traverse claims 47-77 No. 9 is acknowledged. The traversal is on the ground(s) that the method claims necessarily use the product and vice versa and the field of search must necessarily cover both the method class and the product class. This is not found persuasive, because the method invention of claims 47-77 and the product invention of claims 78-87 are distinct inventions as set forth in the Office Action of Paper No. 6, these distinct inventions acquire a separate status in the art as shown by their different classifications and divergent subject matters. The requirement is still deemed proper and is therefore made FINAL.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "a first copper

interconnect comprising a first single via isolated from other vias and an overlying first copper line" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 47-77 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. "forming a (first) copper interconnect to said electrical contact/first copper line through an opening in said (first) insulating layer wherein said (first) copper interconnect comprises a (first) single via isolated from other vias and an overlying first/second copper line" is not supported by specification and figures.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 47-77 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

= With respect to claims 47,

lines 5-7, "forming a first copper interconnect to said electrical contact through an opening in said first insulating layer wherein said first copper interconnect comprises a first single via isolated from other vias and an overlying first copper line" renders the claim indefinite. It is not clear where "a first single via", "other vias" and "an overlying first copper line" are actually located and what relationship of these "a first single via", "other vias" and "an overlying first copper line" corresponds to "an opening in said first insulating layer". It is not clear how a first copper line is considered as "an overlying first copper line" – which element that "a first overlying copper line" overlies on. Moreover, it is not clear that "said first copper interconnect comprises a first single via isolated from other vias and an overlying first copper lines" means that "a first single via" is isolated from both of "other vias" and "an overlying first copper lines" OR "said first copper interconnect comprises a first single via isolated from other vias and an overlying first copper lines" means that "said first copper interconnect" comprises "a first single via", "other vias" and "an overlying first copper lines" wherein only "a first single via" being isolated from "other vias".

Lines 8-9, "forming a slot in said first copper line adjacent to said first single via wherein said slot provides stress relief at an interface of said first single via and said

first copper line" renders the claim indefinite. Limitation of "said first copper line" lacks of antecedent basis – it is not clear where "said first copper line" comes from and is located. In addition, "a slot in said first copper line adjacent to said single via" renders the claim indefinite – it is not clear that "a slot" or "said first copper line" is adjacent to said first single via.

= With respect to claim 48,

lines 3-5, "forming a second copper interconnect through said second insulating layer to said first copper interconnect wherein said second copper interconnect comprises a second single via isolated from other vias and an overlying second copper line" renders the claim indefinite. It is not clear where "a second single via", "other vias" and "a second overlying copper line" are actually located. It is not clear that "other vias" as cited in claim 48 line 5 is the same or different to "other vias" as cited in claim 47 line 7. In addition, it is not clear how a second copper line is considered as "an overlying second copper line" – which element that "a second overlying copper line" overlies on.

= With respect to claim 52,

line 2, it is not clear that "said slot" as cited in claim 52 line 2 is the same to "a slot" as cited in claim 47 line 8 or not.

= With respect to claim 53,

it is not clear how "said slot" (a slot) comprises a first slot, a second slot and a third slot.

= With respect to claim 64,

line 2, it is not clear that "said slot" as cited in claim 64 line 1 is the same to "a slot" as cited in claim 47 line 8 or not. In addition, it is not clear how "said slot" (a slot) comprises a first slot, a second slot and a third slot. Moreover, it is not clear that "a first slot", "a second slot" and "a third slot" as cited in claim 64 lines 6, 4 and 6 respectively the same as "a first slot", "a second slot" and "a third slot" as cited in claim 53 lines 2, 3 and 5 respectively or not.

= With respect to claim 70,

lines 5-7, "forming a copper interconnect to said first copper line through an opening in said insulating layer wherein said copper interconnect comprises a single via isolated from other vias and an overlying second copper line" renders the claim indefinite. It is not clear where "a single via", "other vias" and "an overlying copper line" are actually located and what relationship of these "a first single via", "other vias" and "an overlying first copper line" corresponds to "an opening in said insulating layer". It is not clear that "an overlying copper line" is the copper line which overlies on which element – the first insulating film or the single via or the other vias? Moreover, it is not clear that "said copper interconnect comprises a single via isolated from other vias and an overlying first copper lines" means that "a single via" is isolated from both of "other vias" and "an overlying first copper lines" OR "said first copper interconnect comprises a single via isolated from other vias and an overlying first copper lines" means that "said first copper interconnect" comprises "a single via", "other vias" and "an overlying first copper lines" wherein only "a single via" being isolated from "other vias".

Line 8, "forming a slot in said first copper line adjacent to said first single via " renders the claim indefinite. It is not clear what being adjacent to said first single via – a slot or said first copper line?.

= With respect to claim 71,

it is not clear how "said slot" (a slot) comprises a first slot, a second slot and a third slot. In addition, "said first single via" lacks of antecedent basis – it is not clear where "said first single via" comes from and is located.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 47-54, 56-58, 61-65, 67, 69-72, 74 and 76-77, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Andricacos et al [US 6,090,710] in view of Kazuhiko Kasahara [JP 3-200332].

= With respect to claims 47 and 53-54, Andricacos et al discloses (figs 1-9, col 1-8) method for forming copper interconnects in fabrication of an integrated circuit comprising:

providing a substrate having a point of electrical contact (1st right bottom encapsulated copper alloy line on substrate, fig 8, col 6 lines 14-46) in or on said substrate and having a first insulating layer (first insulator, figs 8); and

forming a first copper interconnect to said point of electrical contact (bottom right 1st encapsulated copper alloy line on substrate, figs 8-9) through an opening in said first insulating layer (figs 9-8) wherein said first copper interconnect comprises a first single via (Cu-alloy connecting to the bottom right 1st encapsulated copper alloy line on substrate through the opening in the first insulator, fig 9) and an overlying first copper line (middle 2nd encapsulated copper alloy line on the first insulator, fig 9), said first single via being located in said opening, said overlying first copper line overlying and being adjacent to said first insulating layer and said first single via.

Andricacos et al does not teach:

a) forming slots in said first copper line wherein said overlying first copper line being adjacent to said first single via, said slots provides stress relief at interface of said first single via and said overlying first copper line ***[claim 47];***

b) wherein said slots comprises a first slot spaced a first distance from said first single via in an X-direction, a second slot spaced a second distance from said first single via in an X-direction opposite from said X-direction of said first slot, and a third slot spaced from the first single via in Y-direction ***[claim 53];*** and

c) wherein said first, second and third slots have a rectangular or square shape ***[claim 54].***

However, Kazuhiko Kasahara teaches forming slots (16, fig 2) comprising a first lot (16) spaced a first distance from a single via (15, fig 2) in an X-direction, a second

slot (16) spaced a second distance from said single via (15, fig 2) in an X-direction opposite from said X-direction of said first slot, and a third slot (16, fig 2) spaced from the single via (15) in Y-direction; wherein said first, second and third slots have a rectangular or square shape. Kazuhiko Kasahara teaches forming said slots in the wide wiring/metal line for reducing stress in said wiring/metal line and lower wirings/metal lines.

Therefore, it would have been obvious for those skilled in the art to modify process of Andricacos et al by forming the first, second and third slots as in **b)** and **c)**, as as taught by Kazuhiko Kasahara, to reduce stress in the overlying first copper line adjacent to the first single via for improving interconnection ability in the integrated circuit. Regarding to **a),** forming first, second and third slots in the overlying first copper line would provide stress relief in the interface of the first single via and the overlying first copper line in the process of Andricacos et al in view of Kazuhiko Kasahara.

= With respect to claim 48, Andricacos et al (fig 9) teaches further: forrming a second insulating layer (second insulator) overlying said first copper interconnect; and forming a second copper interconnect through said second insulating layer to said first copper interconnect wherein said second copper interconnect comprises a second single via (Cu-alloy connecting to the middle 2nd encapsulated copper alloy line in the second insulator, and an overlying second copper line (top 3rd encapsulated copper alloy line), said second single via being located in said second insulator, said overlying second copper line overlying and being adjacent to said second insulating layer and said second single via.

= With respect to claim 51, said slots in said overlying first copper line in the process of Andricacos et al would provide stress relief at the interface of said second single via and said overlying second copper line.

= With respect to claims 52, 64 and 65, Andricacos does not teach:

a') forming other slots in said overlying second copper line wherein said overlying second copper line being adjacent to said second single via, said other slots in said overlying second copper line provide stress relief at interface between said second single via and said overlying second copper line; ***[claim 52]***

b') wherein other slots comprises a first other slot spaced a first other distance from said second single via in an X-direction, a second other slot spaced a second other distance from said second single via in an X-direction opposite from said X-direction of said first other slot, and a third other slot spaced from the second single via in Y-direction ***[claim 64];*** and

c') wherein said first, second and third slots have a rectangular or square shape ***[claim 65].***

However, Kazuhiko Kasahara teaches forming slots (16, fig 2) comprising a first slot (16) spaced a first distance from a single via (15, fig 2) in an X-direction, a second slot (16) spaced a second distance from the single via (15, fig 2) in an X-direction opposite from said X-direction of said first slot, and a third slot (16, fig 2) spaced from the single via (15) in Y-direction; wherein said first, second and third slots have a rectangular or square shape. Kazuhiko Kasahara teaches forming said slots in the wide

wiring/metal line for reducing stress in said wiring/metal line and lower wirings/metal lines.

Therefore, it would have been obvious for those skilled in the art to modify process of Andricacos et al in view of Kazuhiko Kasahara as described in claim 48 by forming the first, second and third other slots as in **b')** and **c')**, as as taught by Kazuhiko Kasahara, to reduce stress in the overlying second copper line adjacent to the second single via for improving interconnection ability in the integrated circuit. Regarding to **a'),** forming first, second and third other slots in the overlying second copper line would provide stress relief in the interface of the second single via and the overlying second copper line in the process of Andricacos et al in view of Kazuhiko Kasahara.

= With respect to claims 70-72, Andricacos et al discloses (figs 1-9, col 1-8) method for forming copper interconnects in fabrication of an integrated circuit comprising:

providing a first copper line (1st right bottom encapsulated copper alloy line on substrate, fig 8, col 6 lines 14-46) over a substrate;

forming an insulating layer (insulator, fig 8) overlying the first copper line;

forming a copper interconnect to said first copper line (bottom right 1st encapsulated copper alloy line on substrate, figs 8-9) through an opening in said insulating layer (figs 9-8) wherein said copper interconnect comprises a single via (Cu-alloy connecting to the bottom right 1st encapsulated copper alloy line on substrate through the opening in the first insulator, fig 9) and an overlying second copper line (middle 2nd encapsulated copper alloy line on the first insulator, fig 9), said single via

being located in said opening, said second copper line overlying and being adjacent to said insulating layer and said single via.

, Andricacos et al does not teach:

a") forming slots in one or more of said first and second copper lines wherein said first and second copper line being adjacent to said single via, said slots provides stress relief at interface of said first single via and one or more of said first and second copper lines ***[claim 70];***

b") wherein said slots comprises a first slot spaced a first distance from said single via in an X-direction, a second slot spaced a second distance from said single via in an X-direction opposite from said X-direction of said first slot, and a third slot spaced from the single via in Y-direction ***[claim 71];*** and

c") wherein said first, second and third slots have a rectangular or square shape ***[claim 72].***

However, Kazuhiko Kasahara teaches forming slots (16, fig 2) comprising a first lot (16) spaced a first distance from a single via (15, fig 2) in an X-direction, a second slot (16) spaced a second distance from said single via (15, fig 2) in an X-direction opposite from said X-direction of said first slot, and a third slot (16, fig 2) spaced from the single via (15) in Y-direction; wherein said first, second and third slots have a rectangular or square shape. Kazuhiko Kasahara teaches forming said slots in the wide wiring/metal line for reducing stress in said wiring/metal line and lower wirings/metal lines.

Therefore, it would have been obvious for those skilled in the art to modify process of Andricacos et al by forming the first, second and third slots as in **b")** and **c"),** as taught by Kazuhiko Kasahara, to reduce stress in one or more of the first and second copper lines for improving interconnection ability in the integrated circuit. Regarding to **a"),** forming slots in one or more of the first and second copper lines would provide stress relief in the interface of the single via and said one or more of said first and second copper lines in the process of Andricacos et al in view of Kazuhiko Kasahara.

= With respect to claims 49-50, 56-58, 61-63, 67, 69, 74, 76 and 77, ranges of the overlying first copper line width, the overlying second copper line width, the first distance, the second distance, the third distance, the first slot dimension, the second slot dimension, the third slot dimension, the first other distance, the second other distance, the third other distance, the first other slot dimension, the second other slot dimension, the third other slot dimension are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious.

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such

criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

3. Claims 55, 59-60, 66, 68, 73 and 75, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Andricacos et al [US 6,090,710] in view of Kazuhiko Kasahara [JP 3-200332] as applied to claims 53, 64 and 71 above, and further in view of Lur et al [US 5,924,006].

= With respect to claims 55, 66 and 73, Andricocos et al in view of Kazuhiko Kasahara substantially discloses the claimed method except teaching that:

d) the third slot overlaps the first slot by a fourth distance, and the third slot overlaps said second slot by a fifth distance ***[claim 55];***

d') the third other slot overlaps the first other slot by a fourth other distance, and the third other slot overlaps said second other slot by a fifth other distance ***[claim 66];***

d") the third slot overlaps the first slot by a fourth distance, and the third slot overlaps said second slot by a fifth distance ***[claim 55];***

However, forming such slots overlapping each other in same metal line for reducing stress has been known in the art. See Lur et al (fig 3) as an evidence that

shows forming slots overlapping on each other (creating narrow trench totally surrounding the metal line to reduce stress).

Therefore, it would have been obvious for those skilled in the art to modify the process of Andricocos et al in view of Kazuhiko Kasahara by forming overlapping slots as being claimed in **d), d')** or **d')**, as shown by Lur et al, to reduce stress in the copper lines as the designed of device being need for maintaining reliability of interconnection.

= With respect to claims 59-60, 68 and 75, ranges of the fourth distance, the fifth distance, the fourth other distance and the fifth other distance are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. *See In re Aller 105 USPQ233, 255 (CCPA 1955); In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

4. Claims 47-77,as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al [US 5,915,201] in view of Chang [US 6,518,173].

= With respect to claims 47-48, and 52, Chang et al (figs 5 and 9, col 1-5) substantially discloses the claimed method of forming a metal interconnects in fabricating integrated circuit comprising steps of:

providing a substrate having a point of electrical contact (15, fig 9, col 4 lines 41-65) in or on said substrate and having a first insulating layer (16);

forming a first metal interconnect to said point of electrical contact (15, fig 9) through an opening in said first insulating layer (16) wherein said first metal interconnect comprises a first single via (18), first other vias (25) and an overlying first metal line (20), said first single via (18) being located in the opening of the first insulating layer (16) and being isolated from said first other vias (25), said overlying first metal line (20) overlying and being adjacent to said first insulating layer (16) and said first single via (18);

forming slots (fig 5) in said first overlying metal line (20) wherein said overlying first metal line (20) being adjacent to said first single via (18), said slots provides stress relief at interface of said first single via and said overlying first metal line (see figs 5 and 9, col 2 lines 7-26, col 3 lines 35-52, col 4 lines 9-58, slots between the first metal line 20 and adjacent to the first single via 18, when reducing stress in the first metal line 20 system, would provides stress relief at interface between said first single via 18 and the overlying first metal line);

forming a second insulating layer (28, fig 9) overlying the overlying first metal line (20);

forming a second metal interconnect through said second insulating layer to said first metal interconnect wherein said second metal interconnect comprises a second single via (32, fig 9), second other vias (45), and an overlying second metal line (40) wherein said second single via (32) being located in the opening of the second insulating layer (28) and being isolated from said second other vias (45), said overlying

second metal line (40) overlying and being adjacent to said second insulating layer (28) and said second single via (28); and

forming other slots in said overlying second metal line (40) wherein said overlying second metal line being adjacent to said second single via, said other slots provides stress relief at interface of said second single via and said overlying second metal line (see figs 5 and 9, col 2 lines 7-26, col 3 lines 35-52, col 4 lines 9-67 and col 5 lines 1-26: Similar to slots and the overlying first 20 in fig 5 and 9, the other slots between the second metal line 40 and adjacent to the second single via 32, when reducing stress in the second metal line 40 system, would also provides stress relief at interface between said second single via 32 and the overlying second metal line 40).

Chang et al does not teach using copper as the metal for forming the metal interconnect which is the copper interconnect with overlying copper lines.

However, Chan teaches advantages of using copper in forming the copper interconnect comprising copper vias and copper lines to provide a better interconnect ability with low resistivities and low cost (see Chang col 1-12 more particularly col 2 lines 19-37).

Therefore, it would have been obvious for those skilled in the art to modify the process of Chang et al by using copper to form the copper interconnect as being claimed, per taught by Chan, to provide a better integrated circuit with reasons given above.

= With respect to claims 51, those skilled in the art would recognize that said slots in said first overlying copper line in the process of Chang et al in view of Chan would

provide stress relief at the interface of said second single via and the overlying second copper line.

= With respect to claims 53 and 55, Chang et al discloses forming slots comprising first, second and third slots respectively spaced a first, second and third distances from the first single via (18) in respectively X-direction, opposite X-direction and Y-direction; wherein the third slot overlaps the first slot by a fourth distance and the third slot overlaps the second slot by a fifth distance (see fig 5 and 9 for details).

= With respect to claims 64 and 65, Chang et al discloses forming other slots comprising first, second and third other slots respectively spaced a first, second and third other distances from the second single via (32) in respectively X-direction, opposite X-direction and Y-direction; wherein the third other slot overlaps the first other slot by a fourth other distance and the third other slot overlaps the second other slot by a fifth other distance (the same concept as figs 5 and 9).

= With respect to claim 70, Chang et al (figs 5 and 9, col 1-5) substantially discloses the claimed method of forming a metal interconnects in fabricating integrated circuit comprising steps of:

providing a first metal line (20,fig 9) over a substrate (10);

forming an insulating layer (28, fig 9) overlying the first metal line (20);

forming a metal interconnect to said first metal line (20) through an opening in said insulating layer (28) wherein said metal interconnect comprises a single via (32), other vias (45) and a metal line (40), said single via (32) being located in the opening of the insulating layer (28) and being isolated from said other vias (45), said overlying

metal line (40) overlying and being adjacent to said insulating layer (28) and said single via (32); and

forming slots (fig 5) in said metal line (40) wherein said second metal line being adjacent to said second single via, said slots provides stress relief at interface of said single via (32) and said second metal line (40) (see figs 5 and 9, col 2 lines 7-26, col 3 lines 35-52, col 4 lines 9-67 and col 5 lines 1-26: Similar to slots and the overlying first 20 in fig 5 and 9, the other slots between the second metal line 40 and adjacent to the second single via 32, when reducing stress in the second metal line 40 system, would also provides stress relief at interface between said second single via 32 and the overlying second metal line 40).

Chang et al does not teach using copper as the metal for forming the metal interconnect which is the copper interconnect with copper lines.

However, Chan teaches advantages of using copper in forming the copper interconnect comprising copper vias and copper lines to provide a better interconnect ability with low resistivities and low cost (see Chang col 1-12 more particularly col 2 lines 19-37).

Therefore, it would have been obvious for those skilled in the art to modify the process of Chang et al by using copper to form the copper interconnect as being claimed, per taught by Chan, to provide a better integrated circuit with reasons given above.

= With respect to claims 71 and 73, Chang et al discloses forming slots comprising first, second and third slots respectively spaced a first, second and third distances from

the single via (32) in respectively X-direction, opposite X-direction and Y-direction; wherein the third slot overlaps the first slot by a fourth distance and the third slot overlaps the second slot by a fifth distance (see fig 5 and 9 for details).

= With respect to claims 54, 65 and 72, it would have been obvious for those skilled in the art to use the first, second and third slots/other slots with a rectangular or square shape in the process of Chang et al in view of Chan. See In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966) (The court held that the configuration of the claimed container was a matter of choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the particular configuration of the claimed container was significant.)

= With respect to claims 49-50, 56-63, 67-69, 74-77, ranges of the overlying first copper line width, the overlying second copper line width, the first distance, the second distance, the third distance, the first slot dimension, the second slot dimension, the third slot dimension, the first other distance, the second other distance, the third other distance, the first other slot dimension, the second other slot dimension, the third other slot dimension *the fourth distance,* the fifth distance, the fourth other distance and the fifth other distance are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. *See In re Aller 105 USPQ233, 255 (CCPA 1955); In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Response to Arguments

5. Applicant's arguments with respect to claims 47-77 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (703) 308-6172. The examiner can normally be reached on Monday-Thursday 8:00 AM - 7:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-3432 for regular communications and (703) 308-7725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thanhha Pham
June 6, 2003

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800